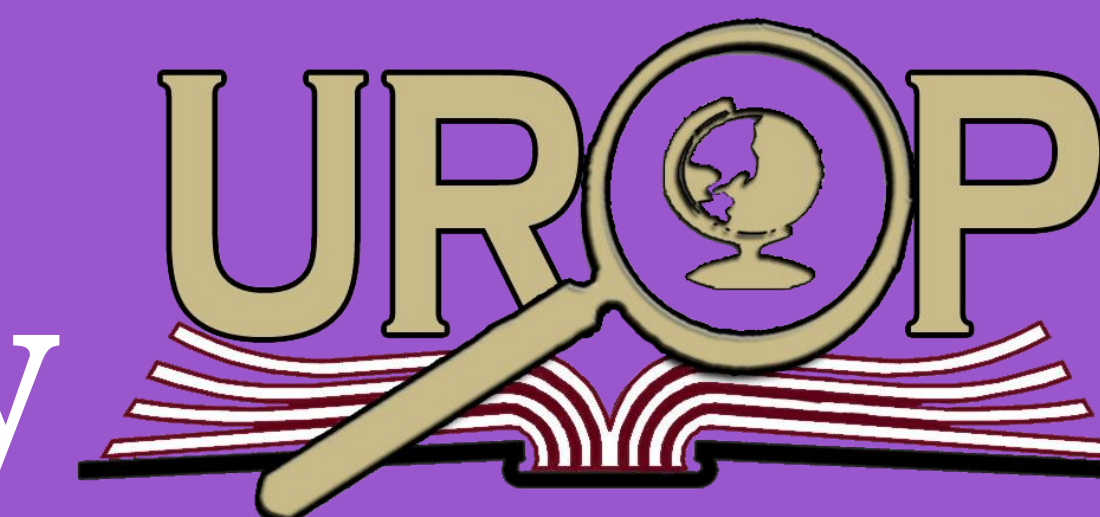




Creating Software for a Scanning Probe Microscopy



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Abstract

We created custom software for a scanning probe microscope (SPM) to support various FSU research projects and experiments. We will begin by giving a brief overview of SPM and its potential applications in scientific research. Following that, we'll talk about why we need specialized software and how it fits our needs. We will also discuss the time and effort required to create this type of machinery. Our presentation will primarily concentrate on the software development process and the key features of the software that we developed. In addition, we will go over the programming languages used for this project and why they were chosen over others.

Introduction

Building a working scanning probe microscopy (SPM) that uses a probe that can scan the surface of a certain element and build an image from that interaction. The probe must be able to magnify and construct the image to a nanoscopic level. Creating a SPM would allow researchers at the National Magnet Laboratory to do important research that requires a microscopy. It would give researchers high resolution images on a nanoscale level on the samples being research on. It could be used in different fields such as materials science, biology, electronics, chemistry, etc., this equipment could be a steppingstone for major innovation.

Methodology

The language the machine software used was Verilog, C++, C, and python. Learning Verilog was extremely difficult as the resource to learn about the language was scarce. Verilog is a low-level language that was used along with some C++ code to run on the machine. It took hours trying to find resources that explained what Verilog was and how to use it. I learned about FPGAs and ASICs as it was associated with the language. It took a while to learn the syntax, planning and designing, and how to optimize the code in Verilog. After learning Verilog, I am now in the process of how to design the software for the microscopy and the way we come at it is through thinking what exactly would be helpful for the researcher to have when running test on the SPM.

```
50 int main(int argc, char **argv) {
51     init(argc, argv);
52
53     int Con,           // Continue option for user
54     P = 3,            // Default P value
55     I = 0,            // Default I value
56     Delay = 20,       // Default Delay value
57     SetPt = 10000,    // Default SetPt value
58     Status = 1,       // Default Status value
59     Option_Picked;    // Option user picked
60
61     do
62     {
63
64         mod = new ModType;
65         Transfer_func = Transfer(150, 0, 2, 1.1, 10, -1);
66
67         mod->clk = 0;
68
69         // Testing this char for P value
70         char Data_Change_S = '0b11010111000010100011110101110000101000111';
71
72         // Default value for P, some type of error where it won't accept any string, int | Try char next time
73         set_value(0b11010111000010100011110101110000101000111, CONTROL_LOOP_P);
74
75         // Default value
76         set_value((V)6 << CONSTS_FRAC, CONTROL_LOOP_I);
77         set_value(Delay, CONTROL_LOOP_DELAY);
78         set_value(SetPt, CONTROL_LOOP_SETPT);
79         set_value(Status, CONTROL_LOOP_STATUS);
80
81         // Menu
82         do
83         {
84             printf("%15s\n", "Menu");
85             printf("(1) Set Control loop P      Current value: %d\n", P);
86             printf("(2) Set Control loop I      Current value: %d\n", I);
87             printf("(3) Set Delay                    Current value: %d\n", Delay);
88             printf("(4) Set setpoint                Current value: %d\n", SetPt);
89             printf("(5) Set status                    Current value: %d\n", Status);
90             printf("(6) Continue\n");
91
92             // Checks for what option user picks
93             scanf("%d", &Option_Picked);
94
95             // Clears unix screen
96             system("clear");
```

Welcome to Verilator

Welcome to Verilator, the fastest Verilog/SystemVerilog simulator.

- Accepts Verilog or SystemVerilog
- Performs lint code-quality checks
- Compiles into multithreaded C++, or SystemC
- Creates XML to front-end your own tools

..	
autoapproach	stuff
control_loop	Add files via upload
raster	raster simulate
spi	correctly (and crudely) simulate control loop
testbench.hpp	stuff
util.hpp	more refactoring

To run the Verilog and C++ code we used a program called Verilator. Verilator tested the software we created and allowed us to debug anything that we needed testing with. This is an extremely important aspect of coding, without testing our code it could lead to vulnerabilities and issues with the software.

Conclusion / Results

Although our study project is still in its early stages, we have made some advancements and are pleased with our results thus far. Within the following years, our group will have finished developing the SPM. Once completed, this hardware will be a useful tool to further the development of other research projects and act as a steppingstone for other researchers in the field. We are eager to carry out this research and observe how it might affect the scientific community.

Acknowledgements

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